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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/561,299

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Jean-Pierre Joly

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05/11/2010

Commissariat a l'Energie Atomique/BHGL

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EXAMINER

ZARNEKE, DAVID A

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/561,299	Applicant(s) JOLY ET AL.	
	Examiner David A. Zarneke	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13, 15-17 and 19-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13, 15-17 and 19-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 2/26/10 with respect to the rejection(s) of the claim(s) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-13, 15-17,19-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kellar et al., US Patent 6,887,769, in view of Suga, US Patent 7,078,811.

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Kellar teaches a method of fabricating a die containing an integrated circuit comprising active components and passive components, the method comprising:

producing a first substrate [110] including at least one active component (3, 14+) and producing a second substrate [120] including critical components (3, 14+);

bonding the first and second substrates, wherein the bonding comprises performing a layer transfer (figure 1B); and

after bonding of the first and second substrates, producing at least one interconnection line [104] between the components of said first and second substrates, said interconnection line passing through the second substrate (Figure 1B).

Kellar fails to teach the second substrate teaches critical passive components.

Suga teaches the second substrate can contain either active or passive components (5, 10+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the passive components of Suga in the invention of Kellar because Suga teaches the conventionality of using either active or passive components on the second substrate. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Kellar and Suga fail to specifically teach at least a part of the passive components comprising critical passive components, wherein production of the critical passive components necessitates the use of a first temperature higher than a second temperature above which the active components are unacceptably degraded and the first substrate is formed using the first temperature.

The claim states that the production of the critical passive components “necessitates” a higher first temperature. Therefore, this higher temperature is inherent to the making of the critical passive components. Which means that the second substrate of Suga comprising only critical passive components inherently has a first temperature higher than a second temperature above which active components are unacceptably degraded.

Regarding claims 2-4, and 17, it would have been obvious to one of ordinary skill in the art at the time of the invention to use transistors as the active components (claim 2); or wherein said critical passive components comprise at least one capacitor and at least one microelectromechanical system (MEMS) (claim 3); or wherein said critical passive components comprise at least one capacitor or at least one microelectromechanical system (MEMS) (claim 4) in the invention of Kellar and Suga because transistors, capacitors, and/or MEMS are commonly known and used active and passive components known to every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

With respect to claims 5-8, and 19, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a dielectric material of said at least one capacitor comprises a perovskite (claim 5); or wherein producing said second substrate comprises producing an electrically conductive material (claim 6); or wherein producing said second substrate comprises producing a dielectric material (claim 7); or wherein producing said second substrate comprises producing perovskite (claim 8) in the invention of Kellar and Suga because a perovskite, an electrically conductive material,

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and a dielectric material are commonly known and used materials known to every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

As to claims 9 and 20, while Kellar and Suga fail to teach producing dielectric insulation trenches in said second substrate during the production of said second substrate, it would have been obvious to one of ordinary skill in the art at the time of the invention to use dielectric insulation trenches in said second substrate in the invention of Kellar and Suga because dielectric insulation trenches in said second substrate are commonly known and used by every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

In re claims 10 and 21, while Kellar and Suga fail to teach producing at least one non-critical passive component during the production of said second substrate, it would have been obvious to one of ordinary skill in the art at the time of the invention to use at least one non-critical passive component during the production of said second substrate in the invention of Kellar and Suga because at least one non-critical passive component during the production of said second substrate is commonly known and used by every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

In re claims 11 and 22, while Kellar and Suga fail to teach producing the non-critical passive component comprises producing a capacitor in trenches, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a

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capacitor in trenches as the non-critical passive component in the invention of Kellar and Suga because a capacitor in trenches is a commonly known and used non-critical passive component to every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Regarding claims 12 and 23, while Kellar and Suga fail to teach producing at least one inductor in the vicinity of a face of the second substrate opposite a bonding face after said bonding of the two substrates, it would have been obvious to one of ordinary skill in the art at the time of the invention to use at least one inductor in the vicinity of a face of the second substrate opposite a bonding face after said bonding of the two substrates in the invention of Kellar and Suga because at least one inductor in the vicinity of a face of the second substrate opposite a bonding face after said bonding of the two substrates is a commonly known and used passive component to every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

With respect to claims 13 and 24, while Kellar and Suga fail to teach producing said at least one inductor on said dielectric insulation trenches, it would have been obvious to one of ordinary skill in the art at the time of the invention to use at least one inductor on said dielectric insulation trenches in the invention of Kellar and Suga because at least one inductor on said dielectric insulation trenches is a commonly known and used passive component to every skilled artisan. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

As to claim 15, Kellar teaches a die fabricated by a method according to claim 1 (the chip system of the abstract).

In re claim 16, Kellar teaches a die containing an integrated circuit comprising active components and passive components and including a single stack of layers, wherein said die comprises an interface between two of said layers such that a first portion of the die [110] situated on one side of said interface includes at least one active component of said active components (abstract), the die comprising at least one interconnection line between the components of said first and second portions, said interconnection line passing through the second portion.

Kellar fails to teach a second portion of said die includes critical passive components of said passive components.

Suga teaches the second substrate can contain either active or passive components (5, 10+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the passive components of Suga in the invention of Kellar because Suga teaches the conventionality of using either active or passive components on the second substrate. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Kellar and Suga fail to specifically teach at least a part of the passive components comprising critical passive components, wherein production of the critical passive components necessitates the use of a first temperature higher than a second

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temperature above which the active components are unacceptably degraded and the first substrate is formed using the first temperature.

The claim states that the production of the critical passive components “necessitates” a higher first temperature. Therefore, this higher temperature is inherent to the making of the critical passive components. Which means that the second substrate of Suga comprising only critical passive components inherently has a first temperature higher than a second temperature above which active components are unacceptably degraded.

With respect to claims 25 and 26, Kellar and Suga teach said active components are disposed in a vicinity of a first face of said die and said die further comprises at least one interconnection line that emerges in the vicinity of said face of said die opposite said first face (figure 1B:[104]).

As to claim 27, while Kellar and Suga fail to teach said at least one inductor and at least one of said interconnection lines are produced during a same process step, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the at least one inductor and at least one of said interconnection lines during a same process step in the invention of Kellar and Suga because the performance of two steps simultaneously, which have previously been performed in sequence was held to have been obvious [In re Tatincloux 108 USPQ 125 (CCPA 1955)].

In re claim 28, while Kellar and Suga fail to teach the second temperature is about 450°C, it would have been obvious to one ordinary skill in the art at the time of the

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invention to optimize the second temperature through routine experimentation (MPEP 2144.05).a

Regarding claim 29, as noted above in the rejection of claim 1, Kellar teaches producing the first substrate comprises producing a substrate including all of the active components of the integrated circuit (3, 14+), and Suga wherein producing the second substrate comprises producing a substrate including only passive components (5, 10+).

With respect to claim 30, while Kellar and Suga, each of which teach an interconnect metal (Kellar:[104] & Suga:[5]), fail to teach producing the first substrate further comprises producing the at least one active component comprising an interconnect metal that may be degraded at the first temperature, the interconnect in both Kellar and Suga “may” degrade at a certain temperature. The word “may” means that it is a possibility that the metal will degrade. The metals used as the interconnects in both Kellar and Suga “may” degrade because they will degrade at a certain temperature.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner, Art Unit 2891
5/8/10